**CONTENT ASSESSMENT 7**

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**Date:** 29-06-2020

**1. Explain in detail the importance of logic-level translations as they apply to I 2C, SPI, and UART busses on the RPi.**

**Ans:**

Logic level translation or voltage translation has become a crucial process in various circuits, in recent years. The mobile applications using several data and application processors make use of low-power CMOS technology that inhibits a supply voltage of less than or equal to1.8 V. The peripheral devices connected to them like RF transceivers, image sensors and memory chips use obsolete and cheaper technologies functioning at high voltage levels of approximately 3V to 5V. Thus, logic level translators allow these devices to connect to each other so that they can work in harmony, without incurring any loss of signals or current flow, thereby enabling efficient system operation and saving power.

**Inter-Integrated Circuit (I2C):**

A multi-master to multi-slave 2-wire serial bus that allows serial communications at several bit rates is termed as I2C (Inter-Integrated Circuit). In order to support several devices with different interface voltage I2C bus systems adapt logic level shifting on the same bus. Since the data rates have hiked from 100 kHz clock rate up to 5MHz in ultra-fast mode, logic level shifting plays a significant role to achieve compatibility with these higher data rates. I2C consists of a single data signal which have their logic levels checked by a clock signal. These two signals are bidirectional and are driven by one or more masters or slaves. Every logic level has its unique logic threshold voltages which helps to find the high or low logic transition. For accurate translation of logic level bidirectional voltage translators can be used to work with I2C bus. It should be carefully noticed that the device forms the exact bus orientation and maps to voltage level of the bus with the correct translator. These devices prove to be excellent for supporting I2C connection between several device interfaces. These bidirectional voltage level translator devices streamline or makes it easy for varied-voltage architectures of the bus enabling, highly versatile solution. They partition the slower and faster elements on an I2C bus, enabling compatibility and interoperability between them. The enable pin of the slower buses can be disabled during fast mode communications. Due to adaptation of high-level frequency they can furnish operations in ultra-fast modes to integrate logic level shifting and provide even greater speeds of I2C interface standards.

**Serial Peripheral Interface (SPI):**

In order to provide synchronous communication between a device peripheral a processor we have serial peripheral interface (SPI). It is a four line “master-slave” communication interface, in which three lines are driven by the processor which is the master and one line driven by the peripheral which is the slave. SPI is widely used in LCD display, sensors, SD cards and memory. To interface different devices using SPI protocol it is extremely important that the signal levels match. When a voltage mismatch is encountered then a level-shifter can be used. The AXC family, SN74AXC4T774 or SN74AVC4T774 gives a favorable mechanism for translation of all four lines used in SPI. The biggest advantage of SN4AXC4T774 is that the channel’s each direction is independently controlled. This proves to be significant in SPI where the three master lines are functioning in opposite direction from one slave line. Serial peripheral interface can house several independent peripheral devices that operate under the same master, the placement of logic level translator becomes crucial. It is suggested to put a logic level translator before every device peripheral if the bus is connected to several multiple peripheral devices on a distinct voltage node.

**Universal Asynchronous Receiver/Transmitter (UART):**

To support two or four signal, asynchronous, full duplex communication we have a hardware device called UART (Universal Asynchronous Receiver/Transmitter). UART is used to convert parallel data to serial data and vice-versa for transmission. A UART that supports two signal communication has host transmit signal and host receive signal, whereas a UART that supports four signal transmission there are host receive signal, host transmit signal along with ready-to-send (RTS) signal and clear-to-send (CTS) signal. RTS and CTS signals are used for handshaking. In order to use UART between two devices functioning at different voltage levels, a voltage translator or logic level translator is important. Either of SN74AXC1T45 or SN74AXC4T245 can be used which can be determined by the configuration of the system. Two SN74AXC1T45 on each data line can be administered for a two-line interface to implement logic level translation. It requires that the direction pin on one device is pulled to VCCA high for translation from A to B and the DIR pin of the other device be pulled to ground for translation from B to A, in this two-line interface configuration. SN74AXC4T245 can be used with DIR1 pin which is pulled to VCCA and the other DIR2 pin which is pulled to ground to achieve voltage translation in a four-line interface configuration. This enables translation of the two channels from A to B and B to A.